

200mW, NPN Small Signal Transistor

FEATURES

- AEC-Q101 qualified
- High current
- Low power loss, high efficiency
- Ideal for automated placement
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-free

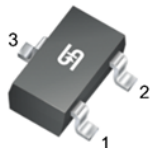
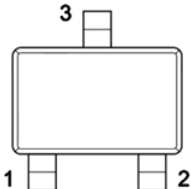
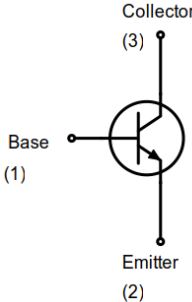
APPLICATIONS

- General switching and amplification

MECHANICAL DATA

- Case: SOT-323
- Molding compound meets UL 94V-0 flammability rating
- Terminal: Matte tin plated leads, solderable per J-STD-002
- Meet JESD 201 class 2 whisker test
- Weight: 5.00mg (approximately)



PACKAGE: SOT-323	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Power dissipation ⁽¹⁾	P _D	200	mW
Collector-base voltage	V _{CBO}	50	V
Collector-emitter voltage	V _{CEO}	45	V
Emitter-base voltage	V _{EBO}	5	V
Collector current	I _C	500	mA
Junction temperature	T _J	-55 to +150	°C
Storage temperature	T _{STG}	-55 to +150	°C

Note:

1. Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TYP	UNIT
Junction-to-ambient thermal resistance ⁽¹⁾	$R_{\theta JA}$	625	°C/W

Thermal Performance Note:

1. Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Collector-base breakdown voltage	$I_C = 10\mu\text{A}$, $I_E = 0\text{A}$	$V_{(BR)CBO}$	50	-	-	V
Collector-emitter breakdown voltage	$I_C = 10\text{mA}$, $I_B = 0\text{A}$	$V_{(BR)CEO}$	45	-	-	V
Emitter-base breakdown voltage	$I_E = 1\mu\text{A}$, $I_C = 0\text{A}$	$V_{(BR)EBO}$	5	-	-	V
Collector-base cut-off current	$V_{CB} = 20\text{V}$, $I_E = 0\text{A}$	I_{CBO}	-	-	0.1	μA
Emitter-base cut-off current	$V_{EB} = 5\text{V}$, $I_C = 0\text{A}$	I_{EBO}	-	-	0.1	μA
DC current gain	$V_{CE} = 1\text{V}$, $I_C = 100\text{mA}$	h_{FE}	160	-	400	-
	BC817-25WH		250	-	600	
	$V_{CE} = 1\text{V}$, $I_C = 500\text{mA}$		40	-	-	
Collector-emitter saturation voltage	$I_C = 500\text{mA}$, $I_B = 50\text{mA}$	$V_{CE(sat)}$	-	-	0.7	V
Base-emitter saturation voltage	$I_C = 500\text{mA}$, $I_B = 50\text{mA}$	$V_{BE(sat)}$	-	-	1.2	V
Base-emitter voltage	$V_{CE} = 1\text{V}$, $I_C = 500\text{mA}$	V_{BE}	-	-	1.2	V
Transition frequency	$V_{CE} = 5\text{V}$, $I_C = 10\text{mA}$, $f = 100\text{MHz}$	f_T	100	-	-	MHz
Output capacitance	$V_{CB} = 10\text{V}$, $I_E = 0\text{A}$, $f = 1\text{MHz}$	C_{obo}	-	5	-	pF

ORDERING AND MARKING INFORMATION

ORDERING CODE	PACKAGE	PACKING	DEVICE MARKING
BC817-25WH RFG	SOT-323	3,000 / 7" Tape & Reel	<u>6</u> B
BC817-40WH RFG	SOT-323	3,000 / 7" Tape & Reel	<u>6</u> C

CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.1 Power Dissipation Curve

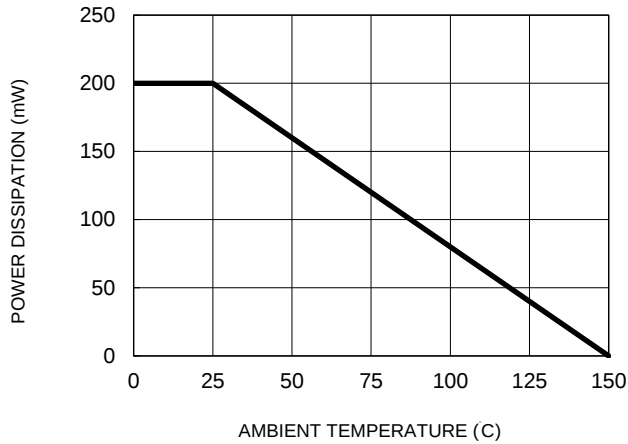


Fig.2 Typical Capacitance Characteristics

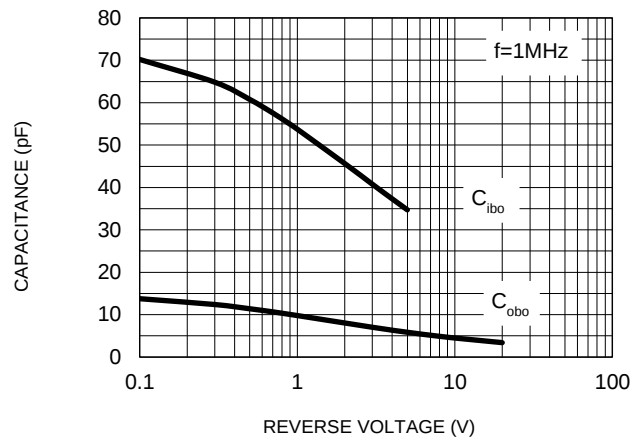


Fig.3 DC Current Gain vs. Collector Current

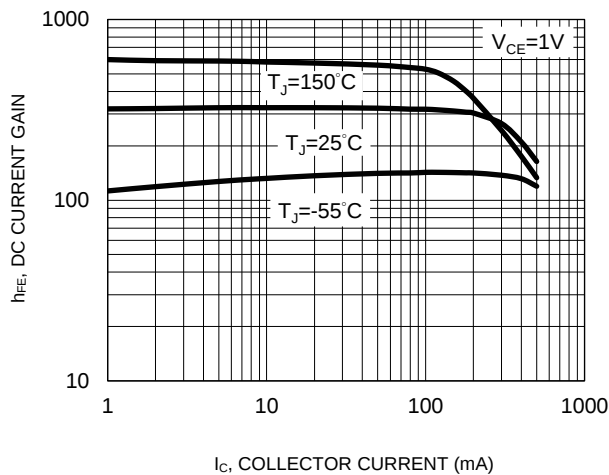


Fig.4 Collector-Emitter Saturation Voltage vs. Collector Current

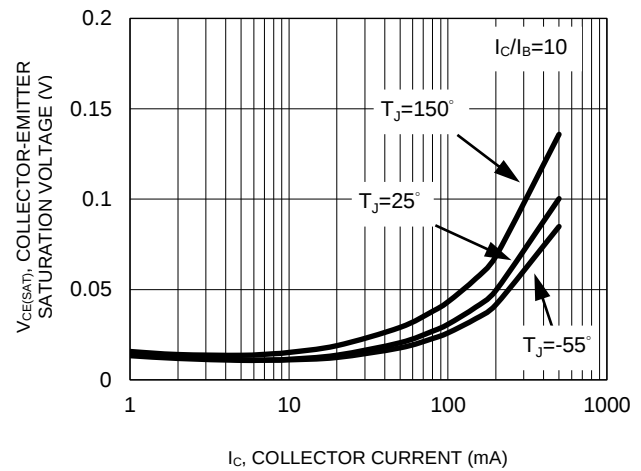


Fig.5 Base-Emitter Saturation Voltage vs. Collector Current

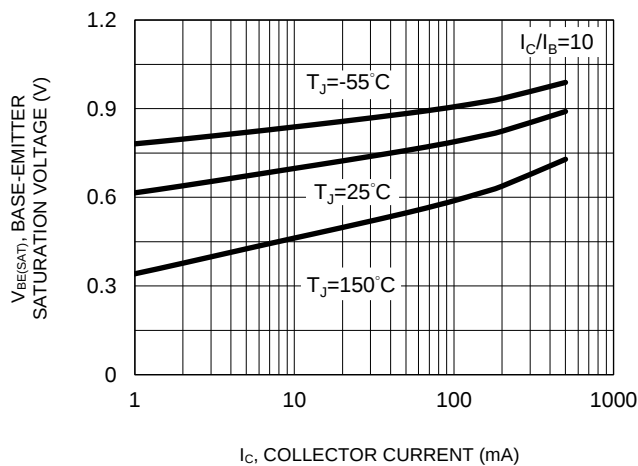
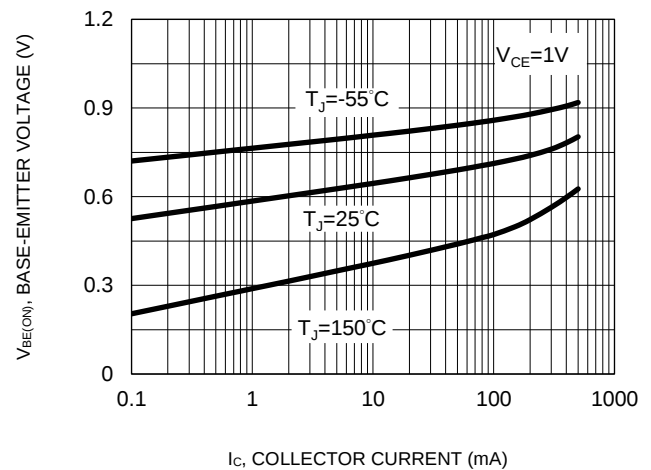
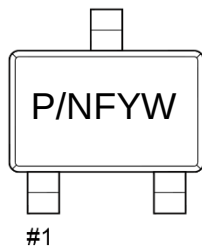
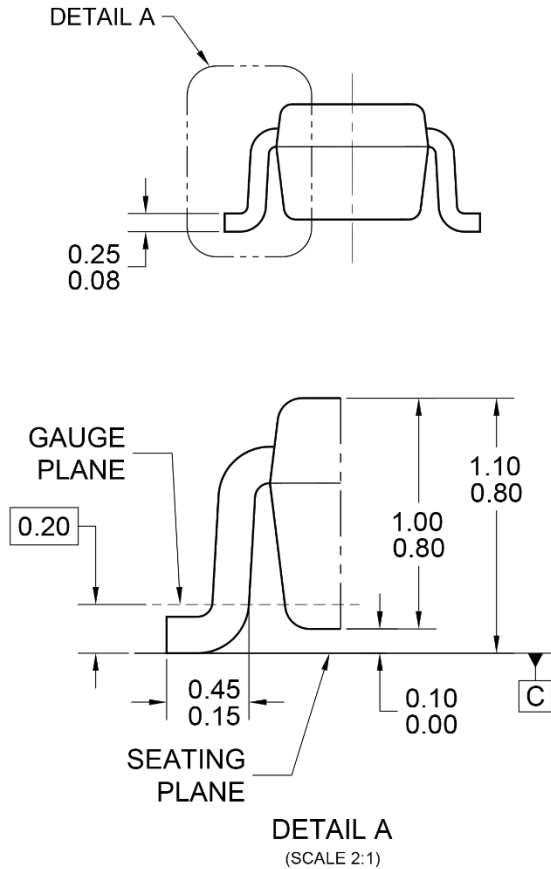
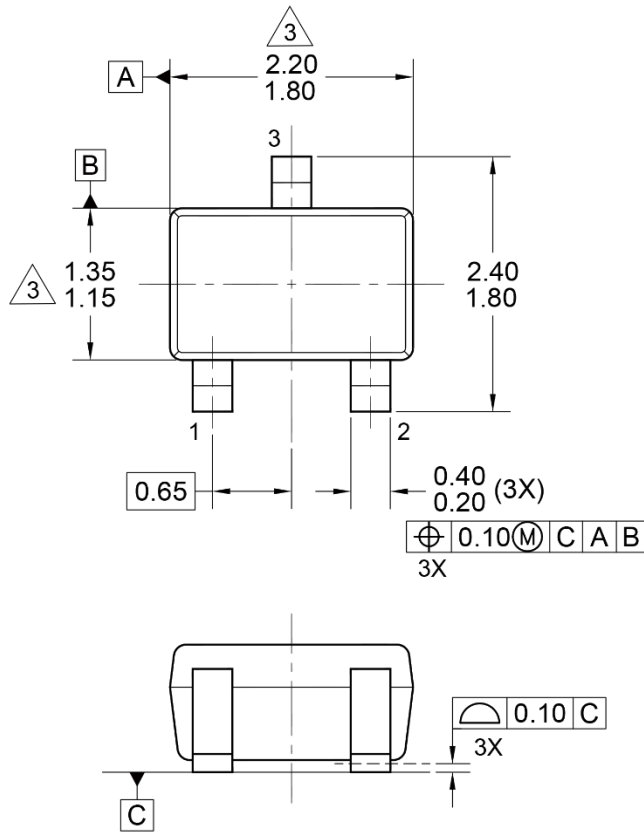


Fig.6 Base-Emitter Voltage vs. Collector Current



PACKAGE OUTLINE DIMENSIONS

SOT-323

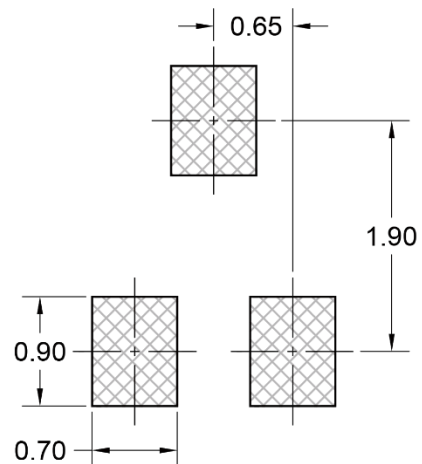


MARKING DIAGRAM

P/N = Device marking Y = Year code
 F = Factory code W = Bi-Week code (A~Z)

NOTES: UNLESS OTHERWISE SPECIFIED

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- PACKAGE OUTLINE REFERENCE: JEITA ED-7500A, EIAJ SC-70.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- DWG NO. REF: HQ2SD07-SOT323-098 REV D.



SUGGESTED PAD LAYOUT

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